

Multicarrier - Based PWM Control Strategies for Five - Level CMLI

R. Banupriya¹, R.Nagarajan², M.Malarvizhi³, M.Dharani Devi⁴

¹Assistant Professor, Department of Electrical and Electronics Engineering, P.G.P. College of Engineering and Technology, Namakkal, India.

²Professor, Department of Electrical and Electronics Engineering, Gnanamani College of Technology, Namakkal, India.

³Associate Professor, Department of Electrical and Electronics Engineering, Gnanamani College of Technology, Namakkal, India.

⁴Associate Professor, Department of Electrical and Electronics Engineering, M.A.M. School of Engineering, Trichy, India.

Abstract – In this paper, performance analysis of different multicarrier pulse width modulation techniques which uses sine (regular) carrier waveforms are carried out for five-level cascaded inverter. In each carrier waveform, different techniques such as phase disposition (PD), inverted phase disposition (IPD), phase opposition disposition (POD) and alternative phase opposition disposition (APOD) are implemented. The fundamental output voltage and harmonics obtained in each method are compared with the output waveform obtained with the triangular carrier waveform. The different PWM methodologies adopting the constant switching frequency multicarrier with different modulation indexes are simulated for a 1kW, 3 ϕ cascaded multilevel inverter using MATLAB/SIMULINK and the effect of switching frequency on the fundamental output voltage and harmonics are also analyzed.

Index Terms – Modulation Index (MI), Sinusoidal Pulse Width Modulation (SPWM), Total Harmonic Distortion (THD),

1. INTRODUCTION

Multilevel inverter is an effective solution for increasing power and reducing harmonics of AC waveform [1]. The elementary concept of a multilevel converter to achieve higher power is to use a series of power semiconductor switches with several lower voltage DC sources to perform the power conversion by synthesizing a staircase voltage waveform. Capacitors, batteries, and renewable energy voltage sources can be used as the multiple DC voltage sources. The commutation of the power switches aggregate these multiple DC sources in order to achieve high voltage at the output; however, the rated voltage of the power semiconductor switches depends only upon the rating of the DC voltage sources to which they are connected [2].

In this paper, constant switching frequency multicarrier pulse width modulation method is used for the multilevel inverter [3]. The control objective is to compare the reference sine wave with multicarrier waves for three phase five level

cascaded inverters. Multilevel voltage source inverter (MVSI) structure is very popular especially in high power DC to AC power conversion applications. It offers several advantages that make it preferable over the conventional voltage source inverter (VSI). These include the capability to handle higher DC link voltage; the stress on each switching device can be reduced in proportional to the higher voltages [4], [5]. Consequently, in some applications, it is possible to avoid expensive and bulky step-up transformer. Another significant advantage of a multilevel output is better sinusoidal voltage waveform. As a result, a lower total harmonic distortion (THD) is obtained [6].

The concept of multilevel converter has been introduced since 1975. The term multilevel began with the three-level converter. Subsequently, several multilevel converter topologies have been developed, such as the Diode Clamped Multilevel Inverter (DCMLI) also known as Neutral Point Clamped (NPC) Inverter, Flying Capacitor Multilevel Inverter (FCMLI) and Cascaded Multilevel Inverter (CCMLI) [7], [8]. Among them, CCMLI topology is the most attractive, since it requires the least number of components and increases the number of levels in the inverter without requiring high ratings on individual devices and the power rating of the CCMLI is also increased [9], [10]. It also results in simple circuit layout and is modular in structure. Furthermore, CCMLI type of topology is free of DC voltage balancing problem, which is a common issue facing in the DCMLI and FCMLI topologies.

Numerous industrial applications have begun to require higher power apparatus in recent years. Some medium voltage motor drives and utility applications require medium voltage and megawatt power level. For a medium voltage grid, it is troublesome to connect only one power semiconductor switch directly [11]. As a result, a multilevel power converter structure has been introduced as an alternative in high power and medium voltage situations. A multilevel converter not only

achieves high power ratings, but also enables the use of renewable energy sources. Renewable energy sources such as photovoltaic, wind, and fuel cells can be easily interfaced to a multilevel converter system for high power application [12]

In motor applications, high dv/dt in power supply generates high stress on motor windings and requires additional motor insulation. Further; high dv/dt of semiconductor devices increases the electromagnetic interference (EMI), common-mode voltage and possibilities of failure on motor. By increasing the number of levels in the output waveform, the switching dv/dt stress is reduced in the multilevel inverter [13], [14]. Multilevel inverters are suitable for power electronics applications such as flexible AC transmission systems, renewable energy sources, uninterruptible power supplies, electrical drives and active power filters [15], [16].

2. CASCADED MULTILEVEL INVERTER

The single-phase structure of three phase five-level cascaded inverter is illustrated in Figure 1. Each separate DC source is connected to a single-phase full-bridge, or H-bridge, inverter. Each inverter can generate three different outputs voltage level, $+V_{dc}$, 0 and $-V_{dc}$, by connecting the DC source to the AC output by different switching combinations of the four semiconductor switches S1, S2, S3 and S4. To obtain $+V_{dc}$, switches S1 and S2 are tuned on, whereas $-V_{dc}$ can be obtained by tuning on switches S3 and S4. By turning on S1 and S3 or S2 and S4, the output voltage is 0. The AC outputs of each of the full-bridge inverter levels are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs [17], [18].

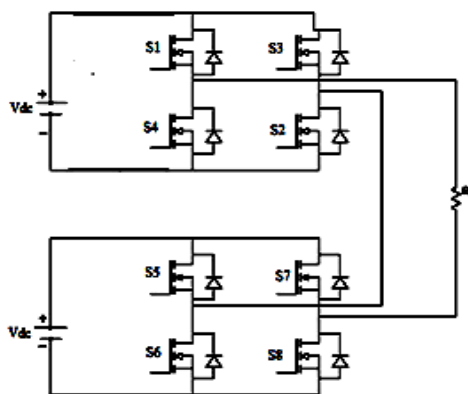


Figure 1, 1 ϕ Structure of Five-Level Cascaded Inverter

The CCMLI is producing five level output and they are $2V_{dc}$, V_{dc} , 0, $-V_{dc}$ and $-2V_{dc}$. This topology is suitable for applications where separate DC voltage sources are available, such as photovoltaic (PV) generators, fuel cells and batteries. The phase output voltage is generated by the sum of two output voltage of the full bridge inverter modules. The circuit in Figure 1 utilizes two independent DC sources and

consequently will create an output phase voltage with five-level. In general, if N is the number of independent DC sources per phase, then the following relations apply [19]:

$$m = 2N + 1 \quad (1)$$

$$q = 2(m - 1) \quad (2)$$

Where m is the number of levels and q is the number of switching devices in each phase. The most well known SPWM which can be applied to a CCMLI is the Phase-Shifted SPWM. This modulation technique is the same as that of the conventional SPWM technique which is applied to a conventional single phase full-bridge inverter, the only difference being that it utilizes more than one carrier. The number of carriers to be used per phase is equal to twice the number of DC voltage sources per phase ($2N$) [20]. The simulation results are obtained for the output phase voltage and line voltage of the three phase five-level CCMLI with 1kW, 3 ϕ resistive loads for various PWM techniques.

3. MODULATION TECHNIQUES

The Pulse Width Modulation (PWM) control strategies development tries to reduce the total harmonic distortion (THD) of the output voltage. Any deviation in the output voltage of the sinusoidal wave shape will result in harmonic currents in the load and this harmonic current produces the electromagnetic interference (EMI), harmonic losses and torque pulsation in the case of motor drives. Increasing the switching frequency of the PWM pattern reduces the lower frequency harmonics by moving the switching frequency carrier harmonic and associated sideband harmonics away from the fundamental frequency component [21], [22]. This increased switching frequency reduces harmonics, which results in a lower THD with high quality output voltage waveforms of desired fundamental RMS value and frequency which are as close as possible to sinusoidal wave shape. The carrier frequency defines the switching frequency of the converter and the high order harmonic components of the output voltage spectrum and the sidebands occur around the carrier frequency and its multiples. The higher switching frequency can be employed for low and medium power inverters, whereas, for high power and medium voltage applications the switching frequency should be low. Harmonic reduction can then be strictly related to the performance of an inverter with any switching strategy [23], [24].

The three phase multilevel inverter requires three modulating signals or reference signals which are three sine-waves with 120 degree phase shift and equal in magnitudes. In this paper, new carrier based PWM techniques are developed which are as Sine Multicarrier Sinusoidal PWM (SMC SPWM).

Each carrier is to be compared with the corresponding modulating sine wave [25], [26]. The reference or modulation

waveform has peak amplitude A_r and frequency f_r and it is centered in the middle of the carrier set. The general principle of a carrier based PWM technique is the comparison of a sinusoidal waveform with a carrier waveform, this typically being a triangular carrier waveform. The reference is continuously compared with the carrier signal. If the reference is greater than the carrier signal, then the active device corresponding to that carrier is switched on, and if the reference is less than the carrier signal, then the active device corresponding to that carrier is switched off [27], [28]. In multilevel inverters, the amplitude modulation index, M_a and the frequency ratio, M_f are defined as,

$$M_a = \frac{A_r}{(m-1)A_c} \quad (3)$$

$$M_f = \frac{f_c}{f_r} \quad (4)$$

Where A_r and A_c are amplitude of reference and carrier signal respectively. f_r and f_c are frequency of reference and carrier signal respectively.

In this paper, modulation indexes used are 0.6, 0.7, 0.8, 0.9 and 1 for five-level CCMLI. For multilevel applications, carrier based PWM techniques with multiple carriers are used. The Multicarrier Modulation (MCM) techniques, can be divided in to the following categories [29], [30] such as,

1. Phase disposition (PD) where all the carriers are in phase.
2. Inverted phase disposition (IPD) where all the carriers are in phase and is inverted.
3. Phase opposition disposition (POD) where the carriers above the zero reference are in phase but shifted by 180 degrees from those carriers below the zero reference.
4. Alternative phase opposition disposition (APOD) where each carrier band is shifted by 180 degrees from the adjacent carrier bands [2].

The above modulation strategies are implemented for sine multicarrier waveform. The phase voltage and line voltage waveform, harmonic spectrums of the line voltage are shown for different modulation techniques by doing simulation using MATLAB/SIMULINK for a five level CCMLI and the results obtained are compared.

3.1. Triangular Multicarrier Sinusoidal PWM (TMC SPWM)

The performance of the multilevel inverter is based on the multicarrier modulation technique used. Two-level to multilevel inverters are made using several triangular carrier signals and one reference signal per phase. Carrara [5] developed multilevel sub harmonic PWM (SH-PWM), which is as follows, for m -level inverter, $m-1$ carriers [31] with the same frequency f_c and same amplitude A_c are disposed such

that the bands they occupy are contiguous. They are defined as

$$C_i = A_c \left((-1)^{f(i)} y_c(\omega_c, \varphi) + t - \frac{m}{2} \right), \quad (5)$$

$$i = 1, \dots, (m-1)$$

Where y_c is a normalized symmetrical triangular carrier defined as,

$$y_c(\omega_c, \varphi) = (-1)^{[\alpha]} ((\alpha \bmod 2) - 1) + \frac{1}{2} \quad (6)$$

$$\alpha = \frac{\omega_c t + \varphi}{\pi}, \omega_c = 2\pi f_c \quad (7)$$

φ represents the phase angle of y_c . y_c is a periodic function with the period $T_c = \frac{2\pi}{\omega_c}$. It is shown that using symmetrical triangular carrier generates less harmonic distortion at the inverters output [32]-[34].

In TMC SPWM, so far only the PD, POD and APOD techniques are discussed earlier in the literature. In this paper, IPD scheme is also applied to TMC SPWM and it is found that this scheme gives the lowest THD among the TMC SPWM schemes.

The multicarrier modulation techniques (PD, IPD, POD and APOD) are implemented using triangular multicarrier signals for five-level CCMLI with different modulation indexes and are shown in Figure 2.

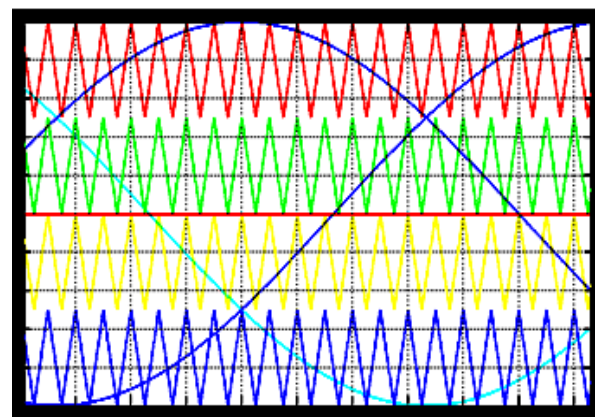


Figure 2 IPD TMC SPWM with $M_a = 1$ for five-level CCMLI

3.2. Sine Multicarrier Sinusoidal PWM (SMC SPWM)

In this PWM technique, the PWM pulses are generated due to the interference of sinusoidal modulating and carrier signals. Here both the modulating and carrier signal are sine wave. The output of the sine wave block in simulink is determined by:

$$y = a \times \sin(f \times t + \phi) + b \quad (8)$$

Where y is the output, a is the amplitude, f is the frequency, t is the time, ϕ is the phase shift and b is the bias. In the gating pulse generation of the proposed SMC SPWM scheme, the triangular carrier waveform of SPWM is replaced by sine waveform. In that the amplitude and frequency of both the signals are differed. The pulses are generated when the amplitude of the modulating signal is greater than that of the carrier signal. The proposed control strategy has a better spectral quality and a higher fundamental output voltage without any pulse dropping.

The multicarrier modulation techniques (PD, IPD, POD and APOD) are implemented using sine multicarrier signals for five-level CCMLI with different modulation indexes and are shown in Figure 3 respectively.

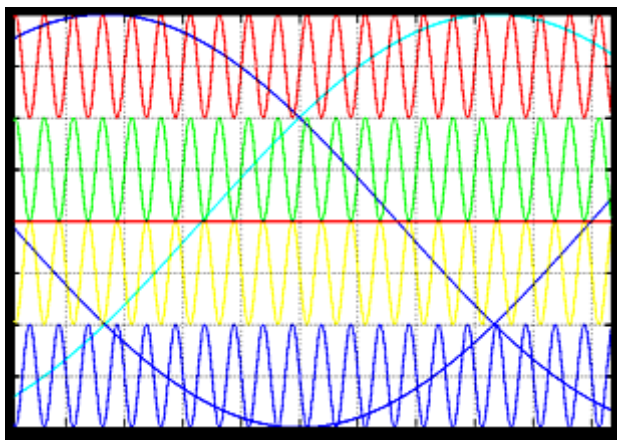


Figure 3 POD SMC SPWM with Ma=1 for five-level CCMLI

4. SIMULATION RESULTS

The five level cascaded multilevel inverter model with different modulation indexes was implemented in MATLAB/SIMULINK software to demonstrate the feasibility of PWM techniques. Phase disposition, inverted phase disposition, phase opposition disposition and alternative phase opposition disposition techniques are used for the various multicarrier SPWM techniques such as;

1. Triangular Multicarrier Sinusoidal PWM
2. Sine Multicarrier Sinusoidal PWM

The line voltage waveform with its harmonic spectrum at fundamental frequency of 50Hz and switching frequency of 2kHz and 10kHz are obtained for the proposed CCMLI. For comparison, the total harmonic distortion (THD) was chosen to be evaluated for all the modulation techniques. In order to get THD level of the waveform, a Fast Fourier Transform (FFT) is applied to obtain the spectrum of the output voltage. The THD is calculated using the following equation in this work [35]-[38].

$$THD = \frac{\sqrt{\sum_{n=2}^{80} v_n^2}}{v_1} \quad (9)$$

Where n is the harmonic order, v_n is the RMS value of the nth harmonic component and v_1 is the RMS value of the fundamental component. Here the %THD is calculated up to a harmonic order which is twice the switching frequency. For 2kHz switching frequency up to 80th order harmonics is taken in to account for calculating THD and for 10kHz switching frequency up to 400th order harmonics is taken in to account for calculating THD.

4.1. Triangular Multi Carrier SPWM (TMC SPWM)

Figure 4(a) and 4(b) show the line voltage waveforms and the percentage THD of the line voltage for five level using the inverted phase disposition technique for triangular multi carrier sinusoidal PWM with Ma=1.

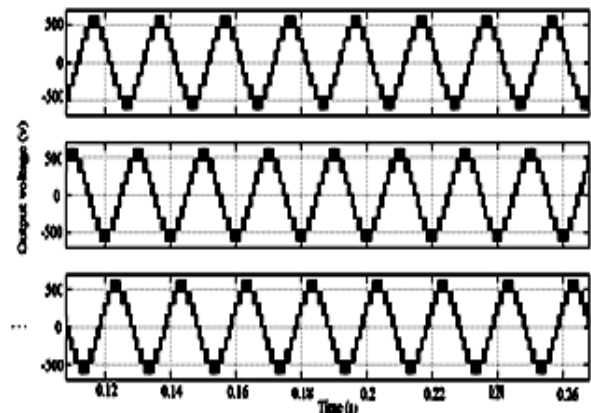


Figure 4(a) Line Voltage for IPD SPWM with Ma=1

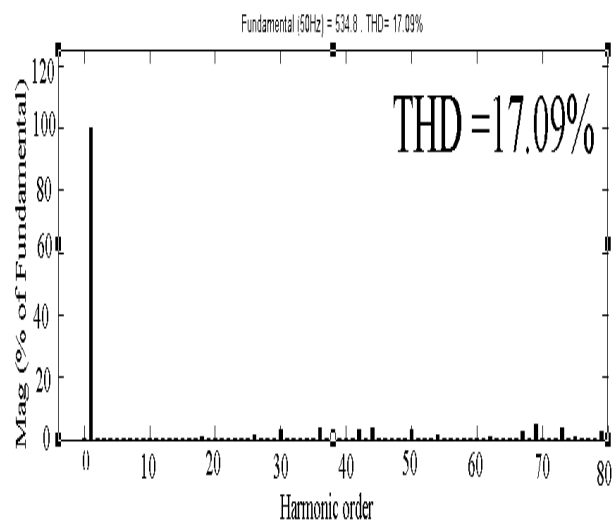


Figure 4(b): Line Voltage %THD for IPD SPWM with Ma=1

Table 1: Line voltage %THD for CCMLI with TMC SPWM

Switching frequency	Modulation Technique	Modulation Indexes				
		$M_a=1$	$M_a=0.9$	$M_a=0.8$	$M_a=0.7$	$M_a=0.6$
2KHz	PD	17.11	17.55	21.73	24.14	25.62
	IPD	17.09	17.55	21.73	24.14	25.62
	POD	21.89	29.94	35.48	38.65	38.42
	APOD	25.66	28.75	29.75	28.04	25.93
10KHz	PD	17.58	17.77	21.81	24.21	28.03
	IPD	17.56	17.77	21.81	24.21	28.03
	POD	23.91	31.42	36.45	38.63	37.68
	APOD	27.07	29.57	30.46	28.85	29.33

Table 1 shows the percentage line voltage THD for the five-level CCMLI with triangular multicarrier signal with different multicarrier PWM techniques with a switching frequency of 2 KHz and 10 KHz respectively for different modulation indexes.

From the above table, it is observed that, when the switching frequency of the CCMLI is increased, the percentage line voltage THD is increased for the PD and IPD schemes with all modulation indexes. In the POD scheme, if the switching frequency is increased, the percentage line voltage THD is reduced with modulation index of 0.7 and 0.6. In the APOD scheme, when the switching frequency is increased, the percentage line voltage THD is increased with all modulation indexes, in five-level CCMLI.

From the simulation result in the triangular multicarrier SPWM technique PD and IPD PWM schemes, from 3rd order harmonics to 25th order harmonics are less than 1%. Few of the odd and even order harmonics from 26th harmonics to 79th harmonics are present. The dominant 69th harmonic factor is about 5% for the PD and IPD schemes. In the POD scheme, from 3rd odd order harmonics to 27th odd order harmonics are less than 1% and all even order harmonics are zero. Few of the odd order harmonics from 29th harmonics to 79th harmonics are 1% to 3%. The dominant 39th and 41st harmonic factor are 10.29% and 10.46% respectively for the POD scheme. In the APOD scheme, from 3rd odd order harmonics to 31st odd order harmonics are less than 1% and all even order harmonics are 0.03%. Few of the odd order harmonics from 33rd harmonics to 79th harmonics are present. The dominant 35th and 45th harmonic factor are 11.94% and 11.87% respectively for the APOD scheme.

4.2 Sine Multi Carrier SPWM (SMC SPWM)

Figure 5(a) and 5(b) show the line voltage waveforms and the percentage THD of the line voltage for five level using the phase disposition technique for sine multi carrier sinusoidal

PWM with $M_a=0.9$.

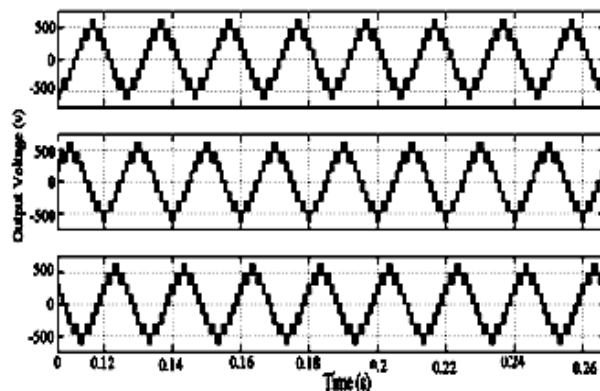


Figure 5(a) Line Voltage for PD SPWM with $M_a=0.9$

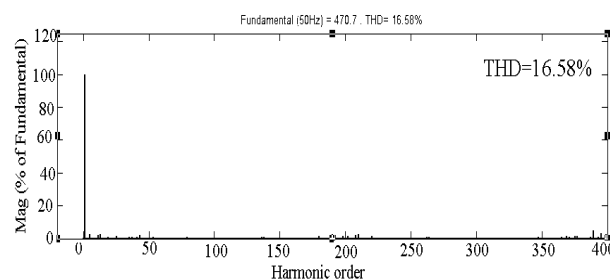


Figure 5(b) Line Voltage %THD for PD SPWM with $M_a=0.9$

Table 2 shows the percentage line voltage THD for the five-level CCMLI with sine multicarrier signal with different multicarrier PWM techniques with a switching frequency of 2kHz and 10kHz respectively for different modulation indexes.

Table 2: Line voltage %THD for CCMLI with SMC SPWM

Switching frequency	Modulation Technique	Modulation Indexes				
		$M_a=1$	$M_a=0.9$	$M_a=0.8$	$M_a=0.7$	$M_a=0.6$
2kHz	PD	17.93	17.25	20.26	23.17	26.68
	IPD	17.93	17.25	20.26	23.17	26.68
	POD	26.34	33.74	38.13	41.82	44.92
	APOD	29.18	31.72	31.57	30.06	27.64
10kHz	PD	18.27	16.58	20.46	22.65	28.68
	IPD	18.27	16.58	20.46	22.65	28.68
	POD	26.15	34.35	37.86	41.14	43.82
	APOD	29.83	32.22	32.19	29.65	29.43

From the above table, it is observed that, when the switching frequency of the CCMLI is increased, the percentage line voltage THD is reduced for the PD and IPD schemes with modulation index of 0.9 and 0.7. In the POD scheme, if the switching frequency is increased, the percentage line voltage THD is reduced with all PWM schemes except for the modulation index of 0.9. In the APOD scheme, when the switching frequency is increased, the percentage line voltage THD is increased with all PWM schemes except for the modulation index of 0.7 in five level CCMLI.

From the simulation result in the PD and IPD PWM scheme, from 3rd order harmonics to 9th order harmonics and higher odd order harmonics (above 9th harmonics) are less than 1%. Few of the even order harmonics from 24th harmonics to 56th harmonics for the above mentioned scheme are less than 2%. The dominant 69th harmonic factor is about 4% for the PD and IPD scheme.

In the POD scheme, from 3rd odd order harmonics to 9th odd order harmonics are less than 1% and all even order harmonics are zero. Few of the odd order harmonics from 11th harmonics to 79th harmonics are 1% to 2%. The dominant 39th and 41st harmonic factor are 13.74% and 13.95% respectively for the POD scheme. In the APOD scheme, from 3rd odd order harmonics to 9th odd order harmonics are less than 1% and all even order harmonics are zero. Few of the odd order harmonics from 11th harmonics to 79th harmonics are present. The dominant 35th and 45th harmonic factor are 12.58% and 12.45% respectively for the APOD scheme.

It is observed that, when the switching frequency of the CCMLI is increased, the percentage line voltage THD, the fundamental phase and line voltage are increased very slightly for the PD and IPD scheme. In the POD and APOD schemes, if the switching frequency is increased, the percentage line voltage THD is decreased very slightly and the fundamental phase and line voltage are increased. Also the fundamental line voltage is maximum for POD and APOD scheme and is minimum for PD and IPD scheme.

5. CONCLUSION

In this paper, the performance of different multicarrier PWM techniques which uses triangular multicarrier waveform, sine multicarrier waveform in multilevel inverters is found out. In all the above PWM techniques, different modulation strategies such as phase disposition (PD), inverted phase disposition (IPD), phase opposition disposition (POD) and alternative phase opposition disposition (APOD) are implemented. The results are verified by doing simulation for a 1kW, three-phase five-level cascaded inverter in MATLAB/SIMULINK. The output quantities like fundamental phase and line voltage, percentage THD of the line voltage and percentage dominant harmonic factor are

measured in the all the above PWM schemes and the results are compared.

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Authors



R. Banupriya received her B.E. in Electrical and Electronics Engineering from Anna University, Chennai, India, in 2010. She received her M.E. Power Electronics and Drives from Anna University, Chennai, India, in 2012. She has worked in the industry as an Asst. Deputy Manager. She is currently working as an Assistant Professor of Electrical and Electronics Engineering at P.G.P. College of Engineering and Technology, Namakkal, Tamilnadu, India. Her research interest includes Power Electronics and Renewable Energy Sources.



R. Nagarajan received his B.E. in Electrical and Electronics Engineering from Madurai Kamarajar University, Madurai, India, in 1997. He received his M.E. in Power Electronics and Drives from Anna University, Chennai, India, in 2008. He received his Ph.D in Electrical Engineering from Anna University, Chennai, India, in 2014. He has worked in the industry as an Electrical Engineer. He is currently working as Professor of Electrical and Electronics Engineering at Gnanamani College of Technology, Namakkal, Tamilnadu, India. His current research interest includes Power Electronics, Power System, Soft Computing Techniques and Renewable Energy Sources.



M. Malarviathi received her B.E. in Electronics and Electronics Engineering from Bharathiyar University, Coimbatore, India. She received her M.E. in Power Electronics and Drives from Anna University, Chennai, India, She received her Ph.D in Electrical Engineering from Anna University, Chennai, India, She has worked in the various institution as an Associate Professor. She is currently working as an Associate Professor of Electrical and Electrical Engineering in Gnanamani College of Technology, Namakkal, Tamilnadu, India. Her research interest includes Power Systems, Power Electronics and Soft Computing.



M. Dharani Devi received her B.E. in Electronics and Instrumentation Engineering from Madurai Kamarajar University, Madurai, India, in 2003. She received her M.E. in Process control and Instrumentation Engineering from Annamalai University, Chidambaram, India, in 2005. She has worked in the various institution as an Associate Professor. She is currently working as an Associate Professor of Electrical and Electronics Engineering at M.A.M.School of Engineering, Trichy, Tamilnadu, India. Her research interest includes Process Control, Power Electronics and Renewable Energy Sources.